polishing (CMP) or grinding. Thus, during the planarization step, the various layers of the film stack are removed. As shown in Fig. 2E, the method of the present invention does not form any substantial divots at either of the STI/substrate corners. Divot formation is substantially phased away in the present invention because the conformal oxide layer formed in the manner indicated above, etches at a slower rate than the trench dielectric material. This differential in etch rate prevents the formation of a divot at the STI/substrate corner. Instead, rounded corners 115 are formed in the present invention, as shown in Fig. 2E.--

**IN THE CLAIMS**

Please amend Claims 28 as follows:

28. (Amended) A semiconductor device comprising at least one substantially planarized trench isolation region formed within a substrate electrically isolating adjacent active device regions from each other, said at least one planarized trench isolation region containing a conformal oxide liner confined within and along sidewalls of said at least one planarized trench isolation region, wherein said conformal oxide liner has rounded corners between a top surface of said substrate and a trench dielectric filling said at least one planarized trench isolation region.

**REMARKS**

Favorable reconsideration and allowance of the claims of the present application, as amended herein, are respectfully requested.

Before addressing the specific grounds of rejection raised in the present Office Action, applicants have amended Claim 28 as well as Page 12, lines 1-15 of the specification of the instant application. Specifically, Claim 28 has been amended to positively recite that the